Listing of Claims

Claims 1-21 cancelled

22. (previously presented) A gate structure with a reduced Voltage threshold (V_{th}) shift comprising:

a high-K gate dielectric layer disposed over a semiconductor substrate; and,

a buffer dielectric layer on the high-K gate dielectric the buffer dielectric layer comprising dopants selected from the group consisting of a metal, a semiconductor, and nitrogen; and,

a gate electrode layer on the buffer dielectric layer.

23. (previously presented) The gate structure of claim 22, wherein the wherein the buffer dielectric layer dopant type and dopant level reduces a Voltage threshold (V_{th}) shift compared to the absence of the doped dielectric buffer layer.

24. (previously presented) The gate structure of claim 22, wherein buffer dielectric layer dopant type and dopant level reduces Voltage threshold (V_{th}) shift less than about half of the

forbidden energy bandgap.

25. (previously presented) The gate structure of claim 22, further comprising an interfacial layer on the semiconductor substrate.

26. (previously presented) The gate structure of claim 25, wherein the interfacial layer is selected from the group consisting of silicon dioxide, nitrided silicon dioxide, silicon nitride and silicon oxynitride.

27. (previously presented) The gate structure of claim 22, wherein the buffer dielectric layer has a dielectric constant of greater than about 3.9.

28. (previously presented) The gate structure of claim 22, wherein the buffer dielectric layer comprises a non-metal containing dielectric selected from the group consisting of semiconductor-oxide, semiconductor-nitride, oxides, nitrides, and silicates.

29. (previously presented) The gate structure of claim 22, wherein the buffer dielectric layer comprises a nitrogen doped dielectric selected from the group consisting of silicon nitrides, silicon oxynitrides, silicate nitrides, and silicate oxynitrides.

30. (previously presented) The gate structure of claim 22, wherein the dopants have a dopant concentration graded in decreasing concentration from the high-K dielectric layer/buffer dielectric layer interface toward the gate electrode layer.

31. (previously presented) The gate structure of claim 22, wherein the buffer dielectric layer comprises a dielectric including metal dopants.

32. (previously presented) The gate structure of claim 31, wherein the dielectric is selected from the group consisting of oxides, nitrides, oxynitrides, silicon oxides, silicon nitrides, silicon oxynitrides, silicate nitrides, silicate oxides, and silicate oxynitrides.

33. (previously presented) The gate structure of claim 31, wherein the metal dopants have a concentration from about 5 atomic percent to about 40 atomic percent.

34. (original) The gate structure of claim 31, wherein the metal dopants are selected from the group consisting of Hf, Al, Ti, Ta, Zr, La, Ce, Bi, W, Y, Ba, Sr, and Pb.

35. (original) The gate structure of claim 31, wherein the metal dopants are selected from the group consisting of Hf and Al.

36. (previously presented) The gate structure of claim 22, wherein different metal dopants comprise PMOS and NMOS gate structures.

37. (original) The gate structure of claim 36, wherein Hf comprises the metal dopants in a NMOS gate structure and Al comprises the metal dopants in a PMOS gate structure.

38. (previously presented) The gate structure of claim 22,

wherein the buffer dielectric layer comprises HfO_2 in a NMOS gate structure and Al_2O_4 in a PMOS gate structure.

39. (previously presented) The gate structure of claim 22, wherein the high-k dielectric layer is selected from the group consisting of metal oxides, metal silicates, metal nitrides, transition metal-oxides, transition metal silicates, metal aluminates, transition metal nitrides, and combinations thereof.

40. (previously presented) The gate structure of claim 22, wherein the high-k dielectric layer is selected from the group consisting of hafnium oxide, aluminum oxide, titanium oxide, tantalum oxide, zirconium oxide, lanthanum oxide, cerium oxide, bismuth silicate, tungsten oxide, yttrium oxide, lanthanum aluminate, barium strontium titanate, strontium titanate, lead zirconate, PST, PZN, PZT, PMN, and combinations thereof.

41. (previously presented) A gate structure with a reduced Voltage threshold (V_{th}) shift comprising:

a semiconductor substrate;

an interfacial layer on the semiconductor substrate;

a high-K gate dielectric layer on the interfacial layer;

a buffer dielectric layer on the high-K gate dielectric the buffer dielectric layer comprising dopants selected from the group consisting of a metal, a semiconductor, and nitrogen; and,

a gate electrode layer on the buffer dielectric layer.

42. (previously presented) A gate structure with a reduced Voltage threshold (V_{th}) shift comprising:

a semiconductor substrate;

a high-K gate dielectric layer on the semiconductor substrate;

a buffer dielectric layer on the high-K gate dielectric the buffer dielectric layer comprising dopants selected from the group consisting of a metal, a semiconductor, and nitrogen; and,

a gate electrode layer on the buffer dielectric layer.